

## **REMARKS**

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove. The Applicants also thank the Examiner for the indication of allowance of Claims 10-17.

Claims 1 - 25 are pending. Of the pending claim set, Claims 1-8 are rejected while Claim 9 is objected to.

Claim 1 positively recites implanting a low dose of nitrogen into the semiconductor substrate in a low voltage core region. These advantageously claimed features are not taught or suggested by the patents granted to Chang et al. or An et al.; either alone or in combination.

The Applicants respectfully traverse the assertion in the Office Action (page 3) that Chang et al. discloses "implanting a low dose of nitrogen (col. 8, lines 34-35) into the semiconductor substrate". The Applicants submit that in the cited column 8 lines 34-35 of Chang et al. an anneal step under nitrogen is disclosed - not a step of implanting nitrogen into a substrate as advantageously claimed.

Regarding Claims 4-5, the Applicants respectfully traverse the assertion in the Office Action (page 3) that Chang et al. discloses the thicknesses of the Applicants' gate dielectric layers. The Applicants submit that Chang et al. discloses a thickness of 70-110Å (e.g. 7-11nm) for the first gate oxide versus the advantageously claimed 7-20Å (e.g. .7-2nm) for the low voltage core gate dielectric. Furthermore, Chang et al. discloses a thickness of 150-190Å (e.g. 15-19nm) for the third gate oxide versus the advantageously claimed .6-2.2nm for the intermediate core dielectric. Lastly, Chang et al. discloses a thickness of 260-300Å (e.g. 26-30nm) versus the advantageously claimed 25-80Å (e.g. 2.5-8nm) for the high voltage gate dielectric.

Regarding Claim 6, the Applicants respectfully traverse the assertion in the Office Action (page 3) that Chang et al. discloses "forming the low voltage core gate dielectric layer...and the intermediate core dielectric layer...in the presence of an environment of nitrogen". The Applicants submit that in Chang et al. the dielectric layers (i.e. elements 40 and 58) are formed (column 8 lines 28-34 and 55-62) before exposure to a nitrogen environment (column 8 lines 34-35 and 62-63); not forming a dielectric layer in the presence of an environment containing nitrogen as advantageously claimed.

Regarding Claim 8 the Applicants respectfully traverse the assertion in the Office Action (page 3) that Chang et al. discloses "forming a second gate over the

low voltage core gate dielectric layer". The Applicants submit that Chang et al. discloses a doped amorphous silicon layer formed over a low voltage gate dielectric layer (FIG. 8), but not implanting nitrogen into the low voltage core region, forming the low voltage gate dielectric, and then forming a second gate over the low voltage core gate dielectric layer as advantageously claimed.

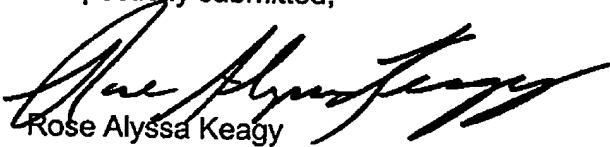
Moreover, the Applicants respectfully traverse the assertion in the Office Action (pages 3-4) that one of ordinary skill in the art would utilize the teachings of Chang et al. and/or An et al. The Applicants submit that one of ordinary skill in the art would not utilize the teachings of Chang et al. because the methods of dry oxidation, wet oxidation, and thermal oxidation taught by Chang et al. could not be used for processing semiconductor substrates which have dielectrics of the thicknesses that are advantageously claimed. Furthermore, one of ordinary skill in the art would not utilize the teachings of An et al. because An et al. does not teach the formation of the advantageously claimed high voltage gate dielectric layer, low voltage core gate dielectric layer, and intermediate core gate dielectric layer. Moreover, one of ordinary skill in the art would not combine the teachings of Chang et al. and An et al. because one of ordinary skill in the art would not combine a process that includes nitrogen implantation (An et al.) with a process that doesn't include nitrogen implantation (Chang et al.). In addition, the methods of Chang et al. for dry oxidation, wet oxidation, and thermal oxidation could not be

used for processing semiconductor substrates which have dielectrics of the thicknesses of An et al.

Therefore, the Applicants respectfully assert that Claim 1 is patentable over the patents granted to Chang et al. and An et al.; either alone or in combination. Furthermore, Claims 2-9 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the references of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



Rose Alyssa Keagy  
Attorney for Applicants  
Reg. No. 35,095

Texas Instruments Incorporated  
P.O. BOX 655474, M/S 3999  
Dallas, TX 75265  
972/917-4167  
FAX - 972/917-4409/4418